AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings of claims in the application:

LISTING OF CLAIMS

1. (Currently Amended) A method for maintaining translation lookaside buffer ("TLB") coherency in a computer system having a plurality of processors, each of the processors having an associated TLB for storing address translation data, the system having a main communication network coupled to the plurality of processors, said method comprising:

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accessing a virtual address in a first TLB ~~an~~ associated with ~~TLB of~~ one of the plurality of processors;

locating an associated physical address corresponding to said virtual address;

performing an operation on the first ~~associated~~ TLB;

generating a TLB message in response to the operation performed on the first ~~associated~~ TLB, if (a) a first entry was input into the first ~~associated~~ TLB when the corresponding associated physical address was not located; (b) a second entry associated with the corresponding associated physical address was moved to another location within the computer system; or (c) the second entry was removed, the TLB message comprising an access request and the associated physical address; ~~and~~

sending the TLB message to the plurality of processors other than the processor associated with the first TLB ~~on which the operation was performed~~ via the main communication network; and

determining, at each of the plurality of processors other than that associated with the first TLB, if the TLB message affects the address translation data stored in the associated TLB in response to receiving the TLB message.

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2. (Previously Presented) The method in accordance with claim 1, wherein the TLB message comprises:

a request for a read access to the first entry to add the address translation data into the associated TLB.

3. (Previously Presented) The method in accordance with claim 1, wherein the TLB message comprises:

a request for a write access to the second entry to modify, remove, or invalidate all copies of the second entry in the associated TLB of each of the plurality of processors.

4. (Currently Amended) The method in accordance with claim 1, wherein said determining comprises ~~further comprising~~:

comparing the first entry with the address translation data in the associated TLB ~~and informing the associated TLB if the first entry affects said address data stored therein~~.

5. (Currently Amended) The method in accordance with claim 4, further comprising:

adding the address translation data for ~~in~~ the first entry into the associated TLB in each of the plurality of processors.

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6. (Currently Amended) The method in accordance with claim 1, wherein said determining comprises ~~further comprising~~:

comparing the second entry with the address translation data in the associated TLB ~~and informing the associated TLB if the second entry affects the address data stored therein~~.

7. (Currently Amended) The method in accordance with claim 6, further comprising:

invalidating the address translation data for ~~in~~ the second entry in the associated TLB in each of the plurality of processors.

8. (Currently Amended) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform a method for maintaining translation lookaside buffer ("TLB") coherency in a computer system having a plurality of processors, each of said processors having an associated TLB for storing address translation data, the system having a main communication network coupled to the plurality of processors, said method comprising:

accessing a virtual address in a first TLB ~~an~~ associated with ~~TLB of~~ one of the plurality of processors;

locating an associated physical address corresponding to said virtual address;

performing an operation on the first ~~associated~~ TLB;

generating a TLB message in response to the operation performed on the first ~~associated~~ TLB, if (a) a first entry was input into the first ~~associated~~ TLB when the corresponding associated physical address was not located; (b) a second entry associated with the corresponding associated physical address was moved to another location within the computer system; or (c) the second entry was removed, the TLB message comprising an access request and the associated physical address; ~~and~~

sending the TLB message to the plurality of processors other than the processor associated with the first TLB ~~on which the operation was performed~~ via the main communication network; and

determining, at each of the plurality of processors other than that associated with the first TLB, if the TLB message affects the address translation data stored in the associated TLB in response to receiving the TLB message.

9. (Currently Amended) An electronic data processing apparatus capable of maintaining translation lookaside buffer ("TLB") coherency, said apparatus comprising:

a plurality of processors;

a plurality of TLBs, each of said plurality of TLBs being connected to and associated with a respective processor of said plurality of processors;

an interconnect network having a plurality of independent paths, each of said plurality of processors distributed among said plurality of independent paths, said plurality of processors being interconnected to each other via a corresponding one of said plurality of independent paths; and

a TLB message generator provided for each of the plurality of processors, said TLB message generator adapted to determine an accessed data address and generate and transmit a TLB message on a corresponding one of said plurality of independent paths, the TLB message comprising an access request and the associated physical address, each of the plurality of processors determining if the TLB message affects the address translation data stored in the associated TLB in response to receiving the TLB message.

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10. (Currently Amended) The apparatus in accordance with claim 9, wherein the TLB message comprises:

a read access request ~~message~~ if the accessed data address is inputted into an associated TLB.

11. (Currently Amended) The apparatus in accordance with claim 9, wherein the TLB message comprises:

a write access request ~~message~~ if the accessed data address modifies, removes, or invalidates the address translation data in an associated TLB.

12. (Currently Amended) A system for maintaining translation lookaside buffer ("TLB") coherency in a computer system including a plurality of processors and a

plurality of TLBs, each of said plurality of TLBs being connected to and associated with a respective processor of said plurality of processors, said system comprising:

an interconnect network having a plurality of independent paths, each of said plurality of processors distributed among said plurality of independent paths, said plurality of processors being interconnected to each other via a corresponding one of said plurality of independent paths;

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means for accessing a data address from one of the associated TLBs;

a TLB message generator for generating a TLB message in response to an operation performed on said one of the associated TLBs, the TLB message comprising an access request and the associated physical address; ~~and~~

means for transmitting the TLB message and the accessed data address to each processor associated with a TLB other than the TLB on which the operation was performed via a corresponding one of the plurality of independent paths; and

means for determining if the TLB message affects the address translation data stored in the associated TLB in response to receiving the TLB message.

13. (Canceled)

14. (Previously Presented) The system in accordance with claim 12, further comprising:

means for adding the accessed data address into the associated TLB in each of the plurality of processors.

15. (Previously Presented) The system in accordance with claim 12, further comprising:

means for invalidating the address translation data in the associated TLB in each of the plurality of processors.

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16. (Previously Presented) The system in accordance with claim 12, further comprising:

means for moving the address translation data in the associated TLB in each of the plurality of processors to another part of the computer system.

17. (Currently Amended) The system in accordance with claim 12, wherein the TLB message ~~further~~ comprises:

a read access request ~~message~~ if the accessed data address is inputted into the associated TLB.

18. (Currently Amended) The system in accordance with claim 12, wherein the TLB message further comprises:

a write access request ~~message~~ if the accessed data invalidates the address translation data in the associated TLB.

19. (Previously Presented) The method in accordance with claim 1, wherein the main communication network includes:

an interconnect network having a plurality of independent paths, the plurality of processors being interconnected to each other via corresponding one of the plurality of independent paths.

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20. (Currently Amended) An apparatus for maintaining translation lookaside buffer ("TLB") coherency in a computer system including a plurality of processors, each of the plurality of processors having an associated TLB for storing address translation data, said apparatus comprising:

means for accessing a virtual address in a first TLB ~~an~~ associated with ~~TLB of~~ one of the plurality of processors;

means for locating an associated physical address corresponding to said virtual address;

means for generating a TLB message in response to the operation performed on the first ~~associated~~ TLB, if (a) a first entry was input into the first ~~associated~~ TLB when the corresponding associated physical address was not located; (b) a second entry associated with the corresponding associated physical address was moved to another location within the computer system; or (c) the second entry was removed, the TLB message comprising an access request and the associated physical address; ~~and~~

means for transmitting the TLB message ~~from the processor associated with the TLB on which the operation is performed~~ to ~~other processors of~~ the plurality of processors other than the processor associated with the first TLB via a plurality of independent paths; and

means for determining, at each of the plurality of processors other than that associated with the first TLB, if the TLB message affects the address translation data stored in the associated TLB in response to receiving the TLB message.

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21. (Currently Amended) The apparatus in accordance with claim 20, wherein said means for transmitting comprises:

means for interconnecting each of the plurality of a processors to one another via corresponding one of the plurality of independent paths.

22 (Previously Presented) The apparatus in accordance with claim 20, wherein the TLB message comprises:

a request for a read access to the first entry to add the address translation data into the associated TLB.

23. (Previously Presented) The apparatus in accordance with claim 20, wherein the TLB message comprises:

a request for a write access to the second entry to modify, remove, or invalidate all copies of the second entry in the associated TLB of each of the plurality of processors.

24. (Currently Amended) The apparatus in accordance with claim 20, wherein said means for determining comprises ~~further comprising~~:

means for comparing the first entry with the address translation data in the associated TLB ~~and for informing the associated TLB if the first entry affects said address data stored therein~~.

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25. (Currently Amended) The apparatus in accordance with claim 24, further comprising:

means for adding the address translation data <u>for</u> ~~in~~ the first entry into the associated TLB in each of the plurality of processors.

26. (Currently Amended) The apparatus in accordance with claim 20, <u>wherein said means for determining comprises</u> ~~further comprising~~:

means for comparing the second entry with the address <u>translation</u> data in the associated TLB ~~and for informing the associated TLB if the second entry affects the address data stored therein~~.

27. (Currently Amended) The apparatus in accordance with claim 26, further comprising:

means for invalidating the address translation data <u>for</u> ~~in~~ the second entry in the associated TLB in each of the plurality of processors.

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28. (New) The method in accordance with claim 1, wherein the system comprises a plurality of independent paths upon which the plurality of processors are distributed and

the main communication network is coupled to the plurality of processors via the plurality of independent paths. said sending comprising:

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sanding the TLB message onto the independent path for the first TLB; and

transmitting the TLB message to respective independent paths of the plurality of processors other than the processor associated with the first TLB via the main communication network.